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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,031	10/30/2001	David A. Kiss	INTO-0011-US (P13281)	7479

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EXAMINER	
CLARK, SHEILA V	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,031	KISS, DAVID A.	
	Examiner	Art Unit	
	S. V. Clark	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-11,13,15-19,21,22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-11,13,15-19,21, 22 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial No: 10/017,031

Art Unit: 2815

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7-11, 13, 15-19, 21, 22, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haba et al in view of Mauritz et al, Hsuan et al (6,236,109) and Kim et al.

Haba et al shows a package integrated circuit comprising processor and a plurality of memory die (see col.1, lines 10-12). As the claims fail to provided specific structure characteristic of a "package", Haba is utilized in this rejection to show specific " package" features (i.e. bus structure, encapsulation 425, substrate 420 including a bus (see figure 4A , 557 having bus connected to wires 556) , chips 440, ball grid array 455, etc.) containing memory chip structure. Long has been the convention in this technology to provide several types of memory devices and processors in a single package to reduce processing costs, package volume, improve signal transmission. The focus of the teachings of Haba et al is a package arrangement that may employ the conventional chips recited in the claims of the instant invention.

Haba et al also clearly teaches the convention of packaging the types of devices including first die, second die, and third die vertically stacked memory structures on a substrate 420 encapsulated (425) in a single package but fails to teach a folded stack and

the specific types of memory claimed. Haba et al also teaches that the vertically stacked memory arrangement more fully optimizes space usage on a printed circuit board substrate (see, col. 4, lines 35-37) and shows said memory die having a distinct electrical connection. It is also however deemed that Haba et al suggests use of conventional memory devices that may be utilized in this art which would include those recited in the claims but however fail to characterize these devices specifically as recited.

Mauritz teaches in figures 1 and 2 integrated circuit packages having plurality of chips including a processor 12, cross point memory in a spare chip 22 and volatile memory 19 and (claim 7) and non-volatile memory chip 16. Mauritz et al also teaches in figure 1 diagram having a first base die 12 as the processor and said memory dies emanating therefrom and vertical thereon and therefore obviously suggesting that said processor may provide a base chip with said memory chips stacked thereon. It would have been obvious to one having ordinary skill in this are that these specific types of devices may be employed in the stacked chip package arrangement of Haba et al because it has long been the convention in this technology to provide several types of memory devices and processors in a single package to reduce processing costs, package volume, improve signal transmission as Hsuan also teaches in col.1, line 35-41. Haba et al in col. 1, lines 10-12, also suggests use of packages having a plurality of memory and processors similar to the structure recited in the claims whereby suggesting said memory may obviously be conventional memory such as volatile memory, cross point and phase change. As discussed above Haba et al further teaches that the vertically stacked memory

arrangement more fully optimizes space usage on a printed circuit board substrate (see, col. 4, lines 35-37).

Folded stacked structures would be further obvious in view of the teachings of Kim et al who shows package chips in folded arrangements. It would have been obvious to one having ordinary skill in this art that the stacked package of Haba et al could be packaged in a folded arrangement because the folded arrangement would allow for an alternative connection to each substrate similar to the connection shown in figure 7D. of Haba et al.

The ball grid array recited in the claims is also taught by Haba and is shown on the bottom surface of substrate 420. Haba et al , Mauritz et al and Kim et al all show bus structures that are typical of package structure.

The invention of Haba et al is deemed to inherently utilize the steps of providing the substrate and die in a vertical stack over the substrate, coupling whereby each die is shown having a separate electrical connection, and packaging whereby all have been discussed above.

Claims 1, 2, 4, 5, 7-11, 13, 15-19, 21, 22, 24-26 are rejected.

Bolken et al, Halahan, Reyes et al, Huppenthal et al, Hoffman et al, Lin et al (6359340) and Lin et al (6461897) are cited to show stacked arrangement of memories and processor in a single package.

Applicant's arguments filed 4-6-2005 have been fully considered but they are not persuasive. The structural features recited in the amended claims are deemed to be substantially addressed in the Board of Appeals Decision rendered 2-4-2005. Applicant

attempts to more specifically address chip structural arrangement whereby said arrangement is not new in stacked chip technology and is further deemed to be taught by Haba et al. Applicant argues that the references relied upon in the rejection fail to show a distinct electrical connection from each of the components claimed but the claims fail to define "distinct" and also fail to characterize it differently than what is taught by Haba et al and the claims further fail to define the "term electrical connection" may have many meanings. Haba et al clearly shows a distinct electrical connection emanating from each device.

Applicant is also to note that stacking chips vertically and having various connection arrangements relative to a lower base substrate is widely taught in this art and that an amended connection arrangement may not necessarily be a novel connection arrangement in stacked chip technology.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.

S. V. Clark
Primary Examiner
Art Unit 2815

June 10, 2005